OIPE
MAR 21 2006
PATENT & TRADEMARK OFFICE

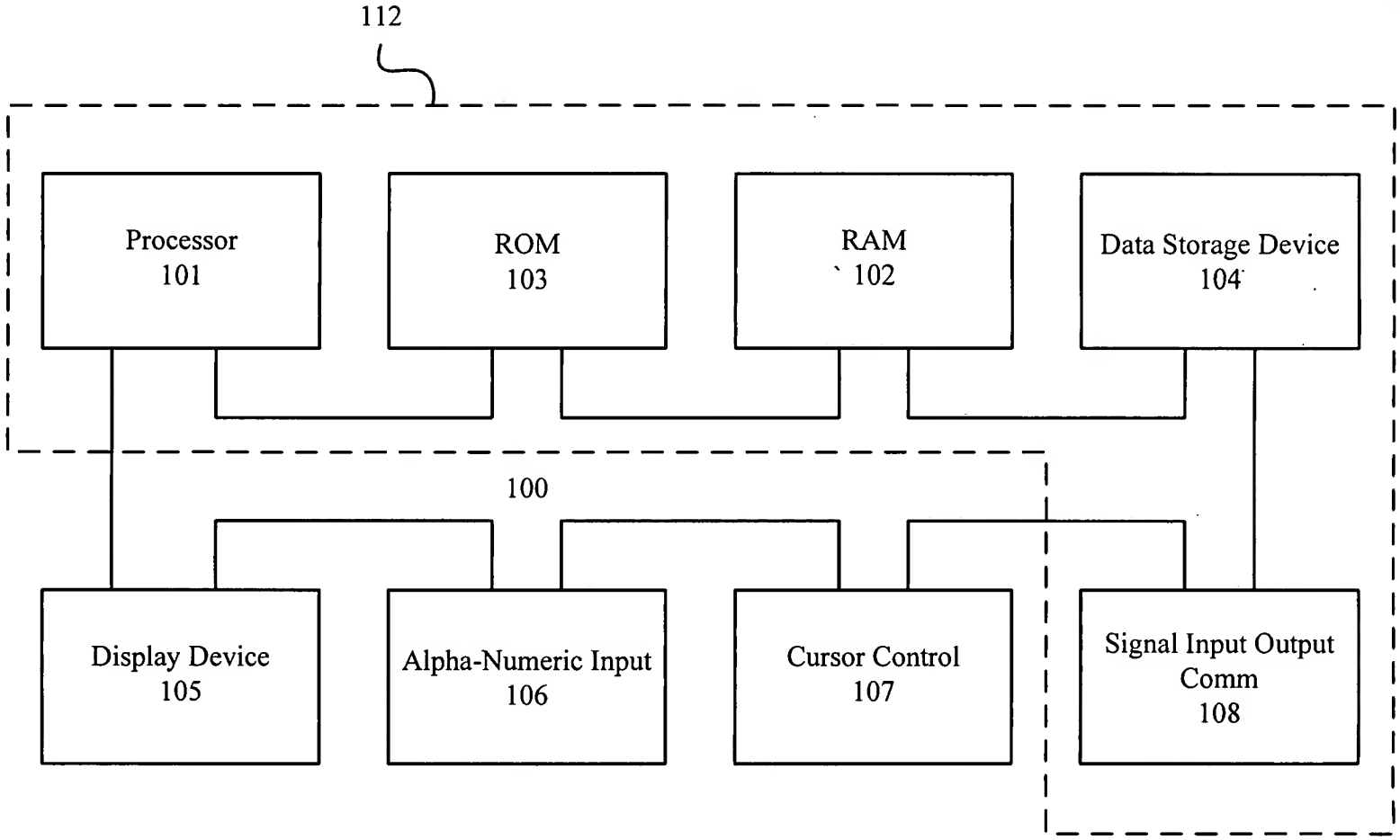

Figure 1

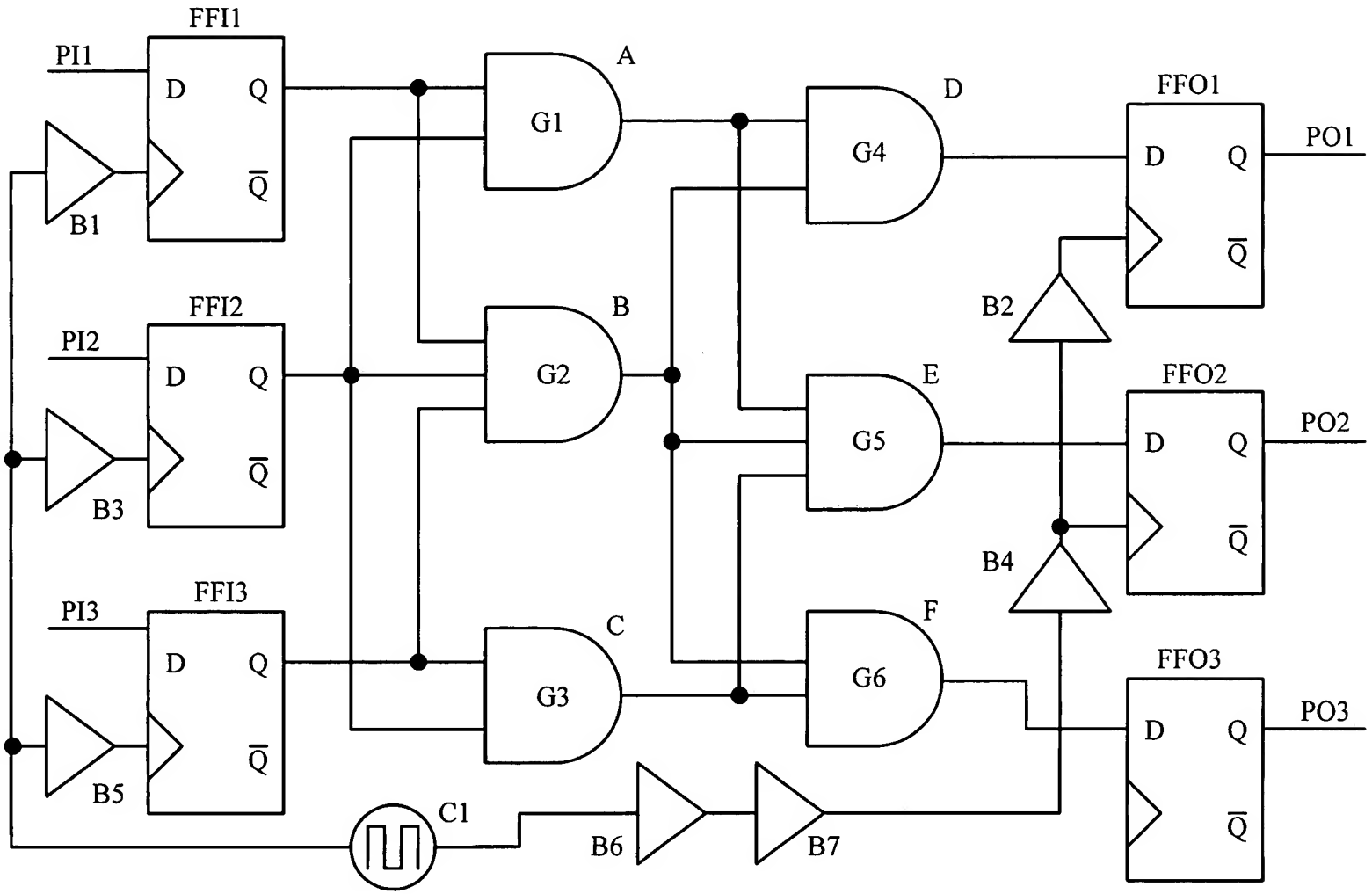
FFI1
PI1
D
Q
Q
B1
FFI2
PI2
D
Q
Q
B3
FFI3
PI3
D
Q
Q
B5
C1
A
G1
B
G2
C
G3
D
G4
E
G5
F
G6
B6
B7
B2
B4
FFO1
D
Q
Q
PO1
FFO2
D
Q
Q
PO2
FFO3
D
Q
Q
PO3

Figure 2A

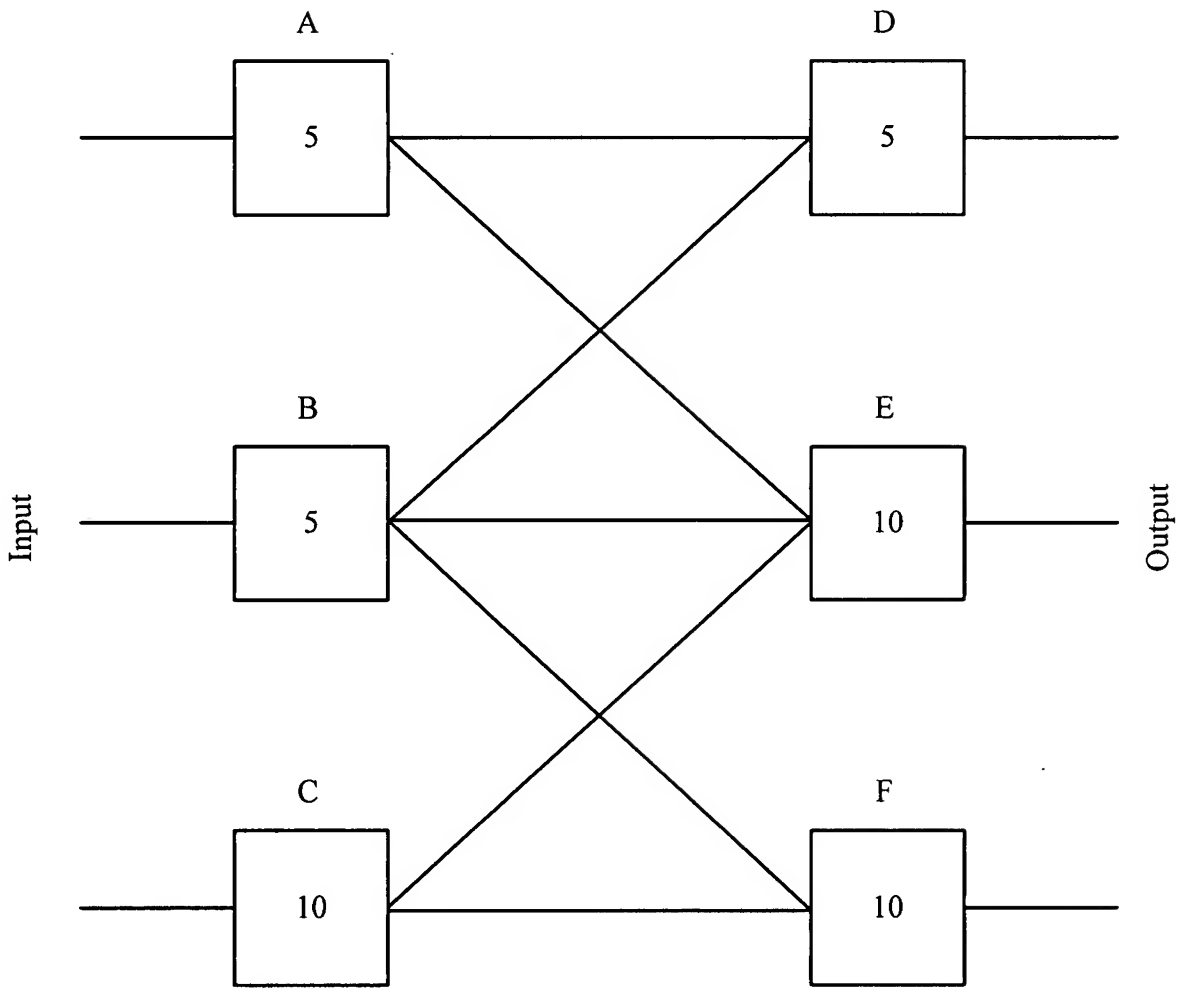

Figure 2B

Forward Delay Sums

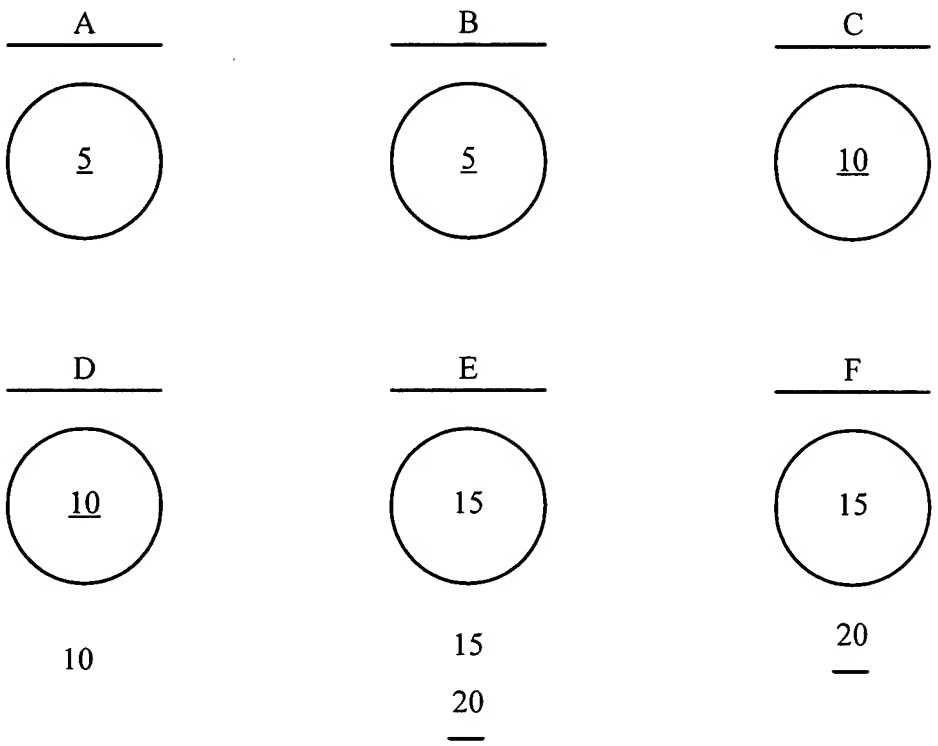

Figure 3

T_{qi}	T_{sj}	T_{hj}	Hold Time Constraint	Minimum Forward Delay Sum	Maximum Forward Delay Sum	Setup Time Constraint	Output Node
2	12	9	7	10	10	26	D
2	3	8	6	15	20	35	E
2	19	10	8	15	20	19	F

Clock Period = 40

Setup Time Constraint = Clock Period – T_{qi} - T_{sj}

Hold Time Constraint = T_{hj} - T_{qi}

Figure 4

Reverse Delay Differences

D	E	F
21	25	9

A	B	C
16	16	15
20	20	-1
	4	

Figure 5

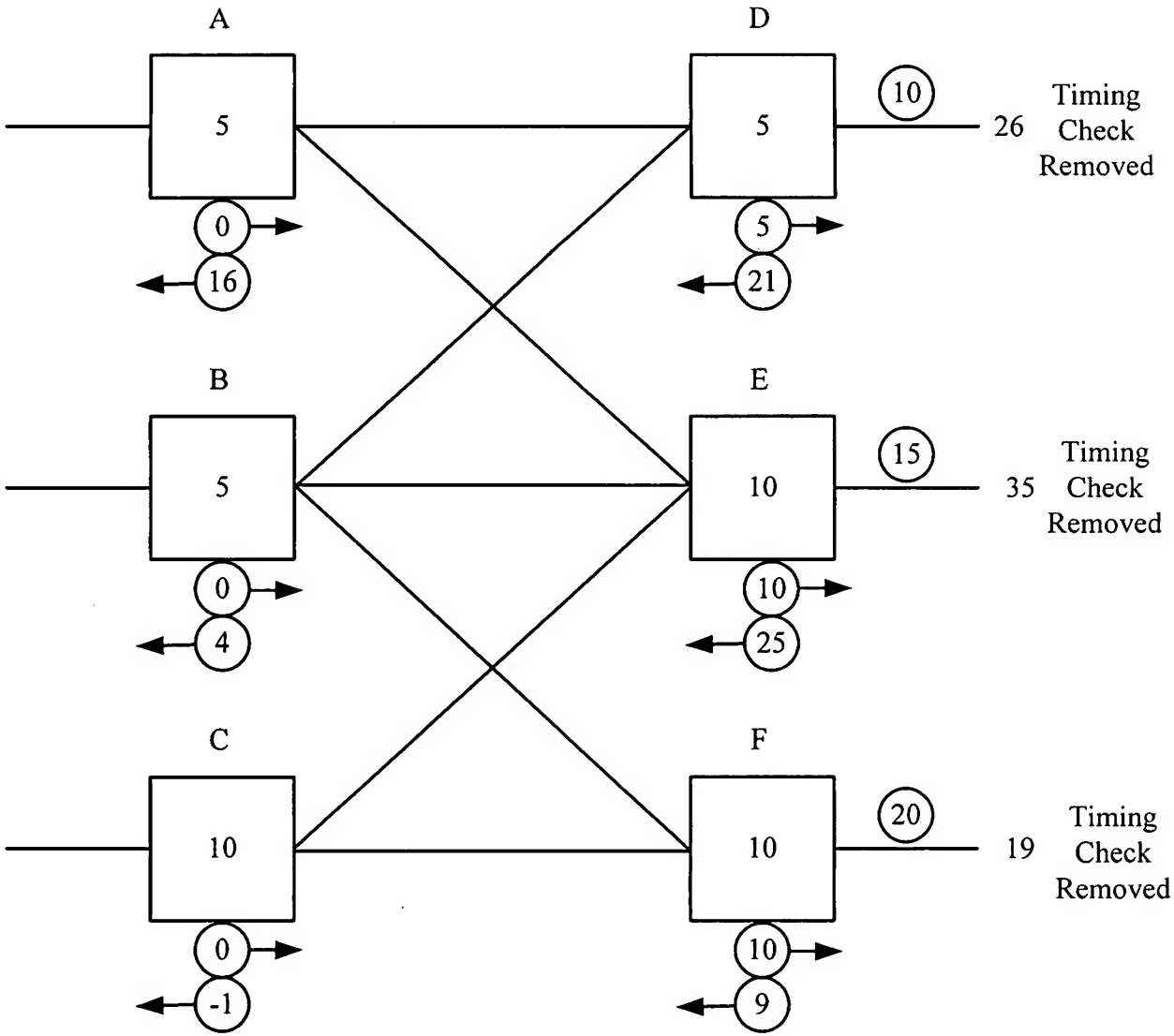
A
5
0
16
B
5
0
4
C
10
0
-1
D
5
5
21
10
26
Timing
Check
Removed
E
10
10
25
15
35
Timing
Check
Removed
F
10
10
9
20
19
Timing
Check
Removed

Figure 6

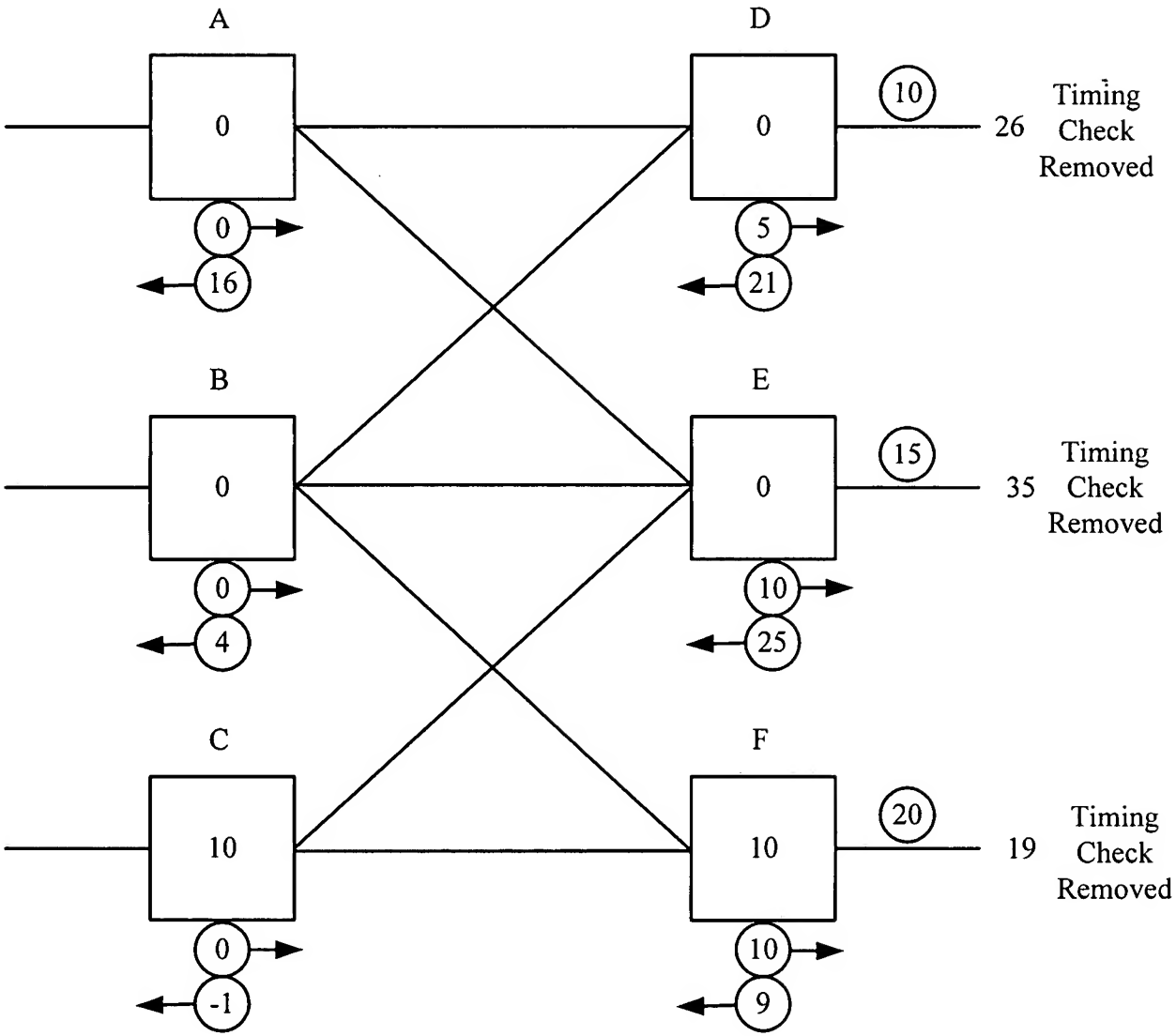
A
0
0
16
D
0
10
5
21
26
Timing
Check
Removed
B
0
0
4
E
0
15
10
25
35
Timing
Check
Removed
C
10
0
-1
F
10
20
10
9
19
Timing
Check
Removed

Figure 7A

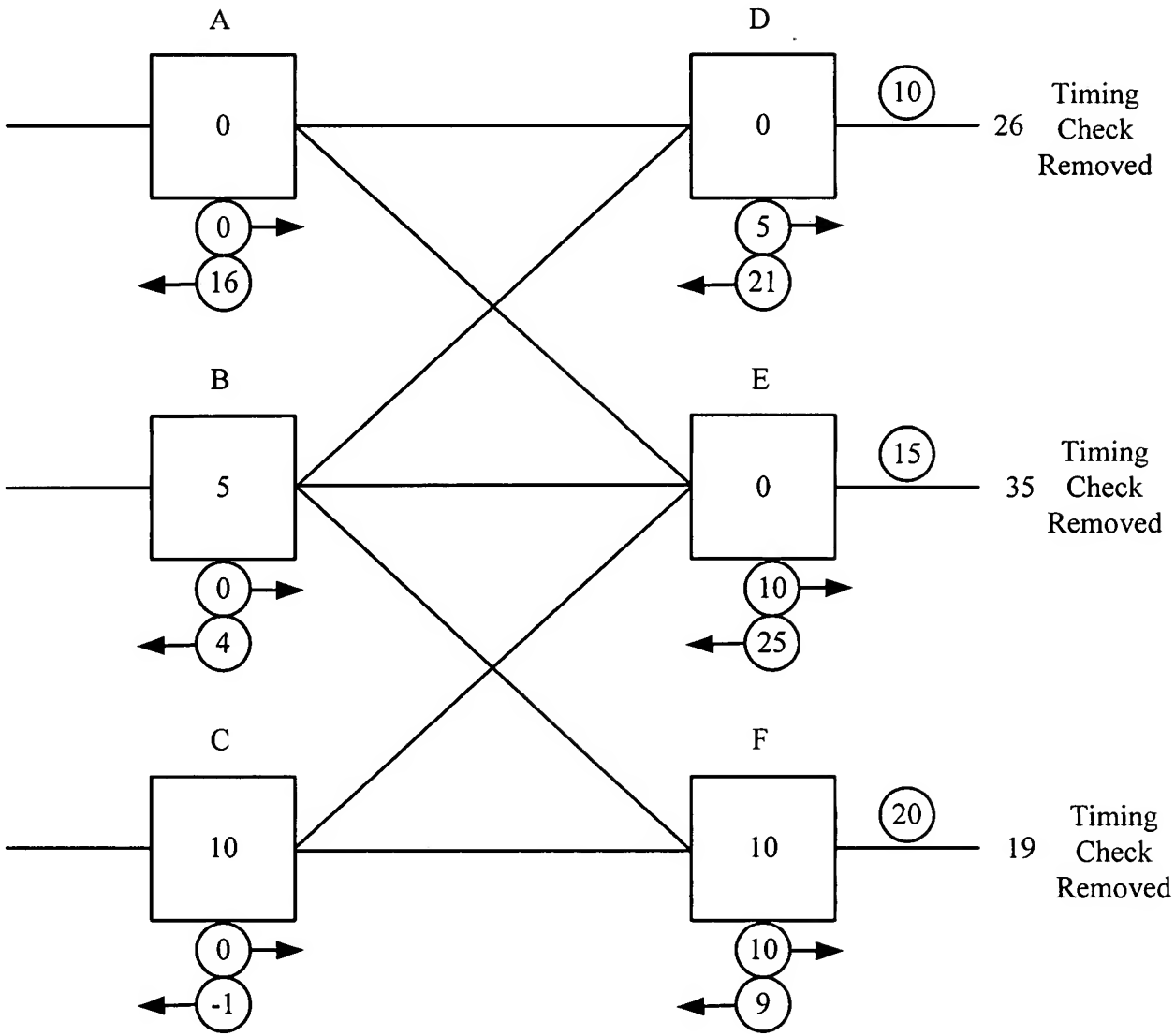
A
D
0
0
10
26
Timing
Check
Removed
0
16
5
21
B
E
5
0
15
35
Timing
Check
Removed
0
4
10
25
C
F
10
10
20
19
Timing
Check
Removed
0
-1
10
9

Figure 7B

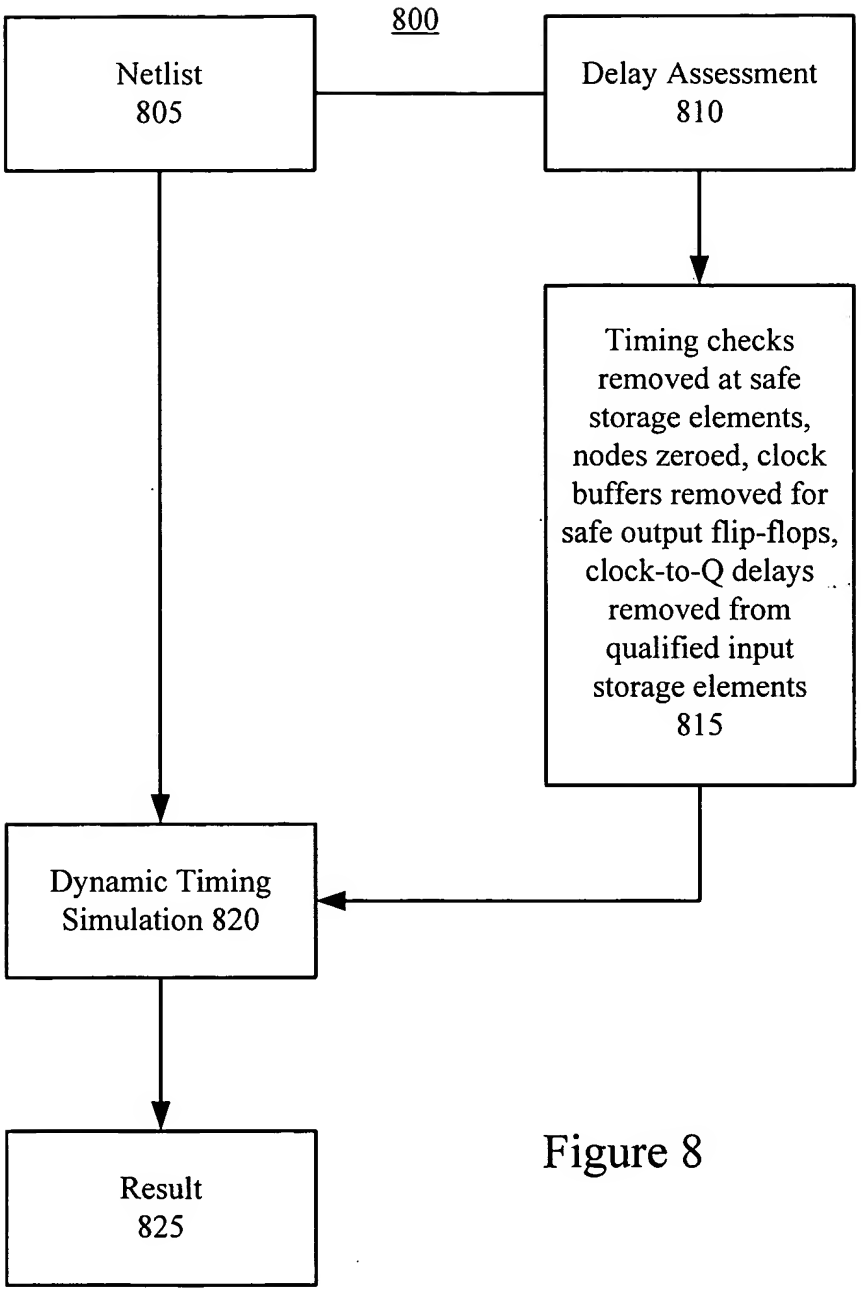
800
Netlist
805
Delay Assessment
810
Timing checks removed at safe storage elements, nodes zeroed, clock buffers removed for safe output flip-flops, clock-to-Q delays removed from qualified input storage elements
815
Dynamic Timing Simulation 820
Result
825

Figure 8

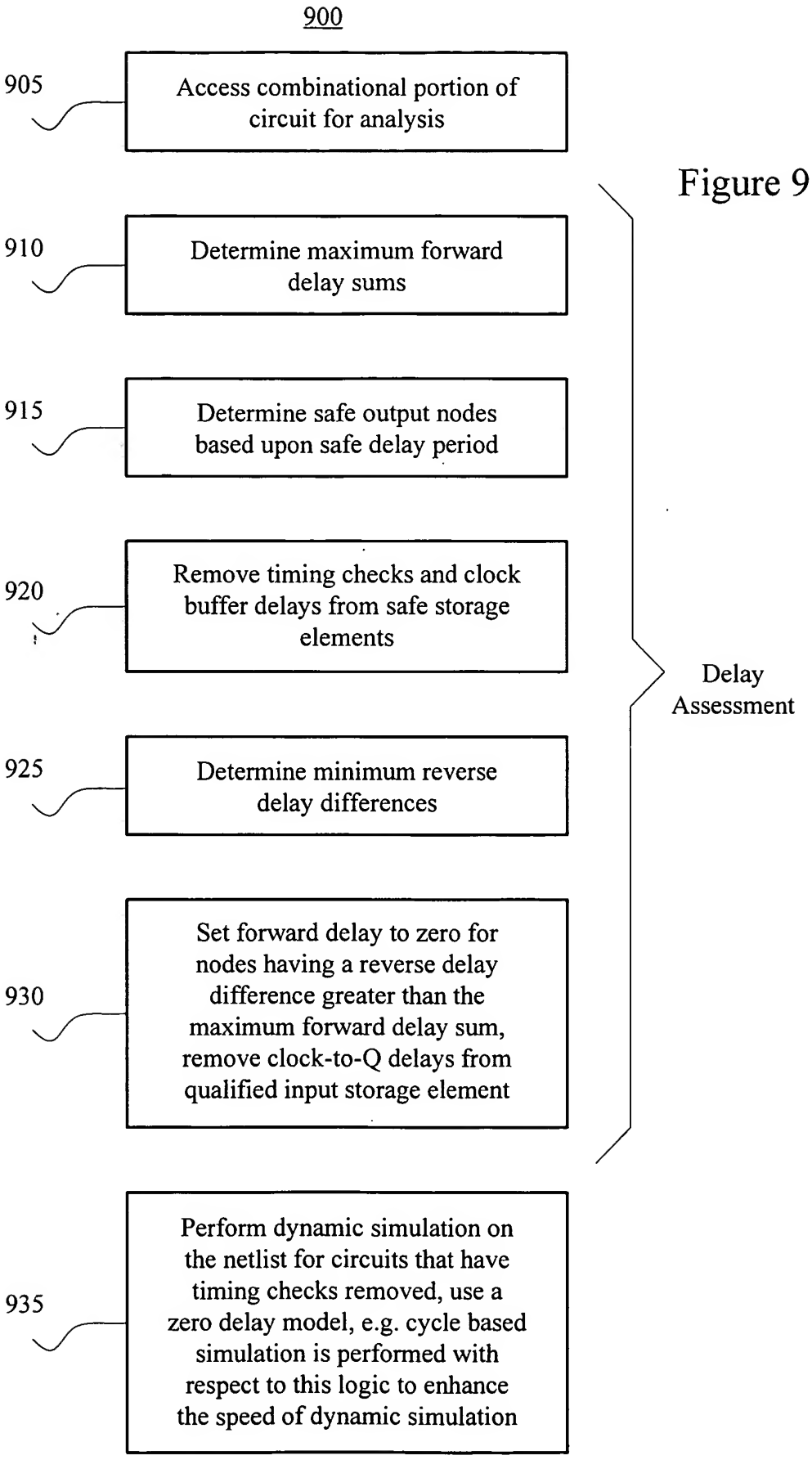
900
905
Access combinational portion of circuit for analysis
910
Determine maximum forward delay sums
915
Determine safe output nodes based upon safe delay period
920
Remove timing checks and clock buffer delays from safe storage elements
925
Determine minimum reverse delay differences
930
Set forward delay to zero for nodes having a reverse delay difference greater than the maximum forward delay sum, remove clock-to-Q delays from qualified input storage element
935
Perform dynamic simulation on the netlist for circuits that have timing checks removed, use a zero delay model, e.g. cycle based simulation is performed with respect to this logic to enhance the speed of dynamic simulation
Delay Assessment

Figure 9